Amendments to the Drawings

Please replace pages 2 and 3 of the previously submitted drawings with the two sheets of amended drawings.

REMARKS

Favorable reconsideration of this application in view of the above amendments and the following remarks is respectfully requested. By this amendment, claims 1, 3, and 4 have been amended to more clearly recite the subject matter of the instant application. Claims 2 and 5 have been canceled without prejudice or disclaimer, and new claim 6 has been added to more fully claim the subject matter of the instant application. Applicant submits that no new matter has been added and formal notice of such is solicited. Currently, claims 1, 3, 4, and 6 are pending of which claim 1 is independent.

FIGS. 3B and 4B have been amended to include the inverted signal $\overline{P}$. The changes to these figures have been marked or circled in red. Acceptance and entry of these two pages is respectfully requested.

The Examiner has objected to the drawings under 37 CFR 1.83(a). In particular, the Examiner believes that the charge-dependent control, formerly recited in independent claim 1, is not shown. Amended claim 1 no longer recites a "charge-dependent control," thereby rendering moot this objection. Accordingly, withdrawal of this objection is respectfully requested.

Claims 1-5 were rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed. Firstly, the Examiner wonders how the signal /P is incorporated with the other signals P, SET, NSET, and PSET with respect to time since it is not shown in FIGS. 3B and 4B. It is well understood that /P is the inverted signal of signal P. Further, FIGS. 3B and 4B have been amended to include the inverted signal /P.

The Examiner also wonders whether the charge-dependent control at page 4, lines 3-5, of the specification, and recited in claim 1, is a circuit, a means, or a signal, as the Examiner believes it is not shown in the drawings. As noted above, claim 1 has been amended to render this issue moot. Therefore, Applicants submit that the subject matter of the instant application is described in a manner that satisfies the enablement requirement. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 1 is rejected under 35 USC 112, second paragraph, for indefiniteness. The Examiner does not believe that there is antecedent basis for the "charge-dependent control."

Claim 1 has been amended, as presented above. Applicants note that the offending phrase is no longer used in the claim, as amended. Therefore, Applicants submit that claim 1, as amended, is not indefinite. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-5 were rejected under 35 USC 102(b) as anticipated by Iida et al., US Patent No. 6,493,282 (hereinafter, Iida '282). This rejection is respectfully traversed.

Independent claim 1 sets forth an integrated memory that includes a memory cell array with word lines for selecting memory cells and bit lines for reading out or writing data signals, a read/write amplifier connected to the bit lines for assessing and amplifying data signals, and a voltage generator circuit. The voltage generator circuit includes a first capacitor, a first transistor with a first terminal connected to an electrode of the first capacitor and a second terminal connected to a first supply potential, a second transistor with a first terminal connected to the electrode of the first capacitor and a second terminal connected to a first terminal of the read/write amplifier, and a pulse shaper connected to a control terminal of the first transistor and a control terminal of the second transistor. The pulse shaper controls the first and second transistors such that the first transistor operates as an open switch and the second transistor operates as a closed switch for a predetermined period of time during an assessment and amplification operation of the read/write amplifier.

Iida '282 relates to a semiconductor integrated circuit includes a first n-well in a p-type semiconductor region, word lines, data lines, a DRAM array, a row of sense amplifiers coupled to the data lines, and a power supply circuit. In Iida '282, a primary internal supply voltage VDD is applied to the sense amplifiers. The power supply circuit, which has no capacitors, sets the primary internal supply voltage at a constant voltage.

Iida '282, however, does not describe or suggest the claimed subject matter of the instant application. For example, as to independent claim 1, Iida '282 lacks a voltage generator that includes a capacitor with an electrode connected to a read/write amplifier and that the voltage generator is not connected to a power supply potential during a predetermined period of time during an assessment and amplification operation of the read/write amplifier. Therefore, Iida '282 fails to teach or suggest the subject matter of independent claim 1. Likewise, Iida '282 fails

to teach or suggest the subject matter of claims 3, 4, and 6, which depend therefrom. Accordingly, withdrawal of this rejection is respectfully requested.

Applicant submits that all pending claims, claims 1, 3, 4, and 6, are in condition for allowance, and formal notice of such is solicited. If the Examiner has any questions, the Examiner is respectfully requested to contact the undersigned at the number listed below.

It is believed that no fees are required at this time. However, Applicant hereby petitions for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Respectfully submitted,

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